DTμL 931 CLOCKED FLIP-FLOP

FAIRCHILD DIODE-TRANSISTOR MICROLOGIC

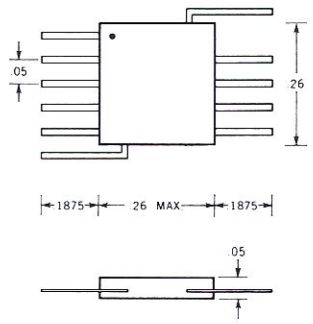
GENERAL DESCRIPTION - The Fairchild Diode-Transistor Clocked Flip-Flop is one of a set of compatible, integrated, logic building blocks designed for low-power and high immunity to noise from -55°C to +125°C. Other DTμL elements are the 930 Dual Gate, the 932 Buffer, and 933 Input Extender.

The 931 Clocked Flip-Flop features an AND gate input permitting operation in either the R-S or J-K mode. The 931 element consists of two flip-flops connected as a "master-slave" combination, thus eliminating the need for capacitors or other circuit delay elements. The "master" flip-flop stores the input information when the clock voltage is high and transfers it to the "slave" when the clock voltage is low. Direct (unclocked) set and clear inputs are also provided.

For complete test conditions and limits, refer to DTμL Composite specification. Refer also to specifications on DTμL 930 Dual Gate, DTμL 932 Dual Buffer, DTμL 933 Dual Extender, DTμL 944 Dual Power Gate, and DTμL 946 Quad Gate.

TYPICAL FLAT PACKAGE

TOP VIEW



R-S MODE TRUTH TABLE

t_n				t_{n+1}
S_1	S_2	C_1	C_2	Q
0	X	0	X	Q_n
0	X	X	0	Q_n
X	0	0	X	Q_n
X	0	X	0	Q_n
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	Undetermined

X - Either a one or a zero can be present

"1" more positive than "0"

For J-K Mode Operation:
Connect S_1 to $\overline{Q}$ and C_1 to Q

J-K MODE TRUTH TABLE

t_n		t_{n+1}
S_1	C_1	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

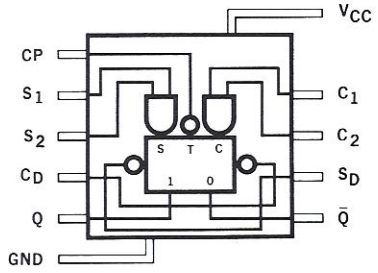
"1" more positive than "0"

For J-K Mode Operation:

Connect S_2 to $\overline{Q}$ and

C_2 to Q

FLAT PACKAGE



(Top View)

Input Load Factor *

CP	2
S_1, S_2, C_1, C_2	2/3

* DTμL 930 Dual Gate Input = 1

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A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

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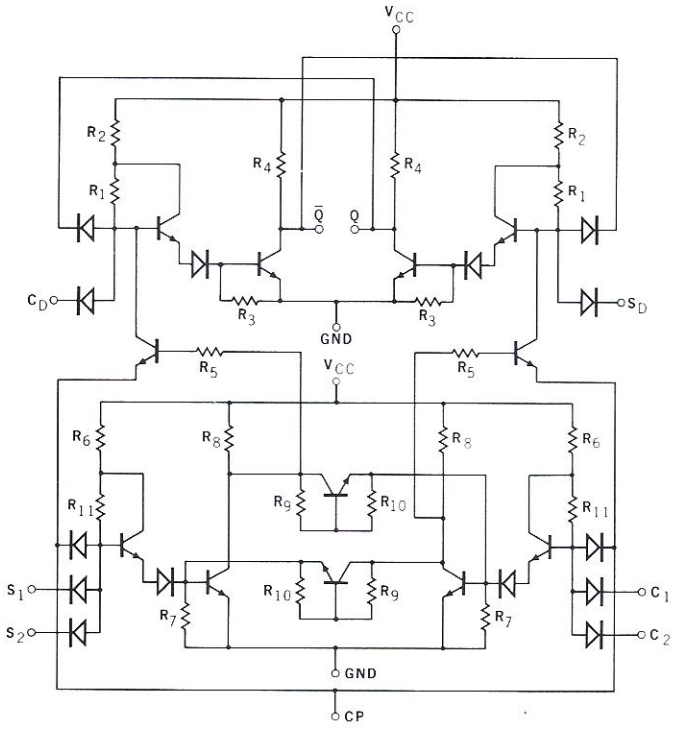
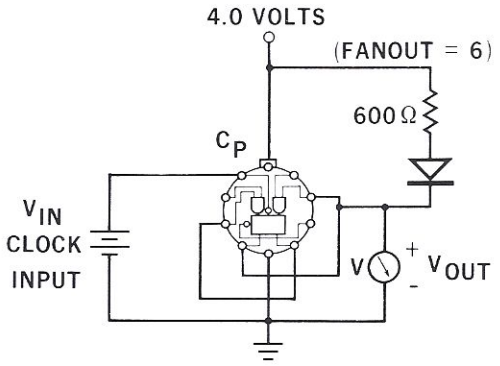
MANUFACTURED UNDER ONE OR MORE OF THE FOLLOWING U. S. PATENTS: 291877, 3015048, 3025589, 3064167, 3108359, 3117260; OTHER PATENTS PENDING.

FAIRCHILD DIODE-TRANSISTOR MICROLOGIC DTμL 931

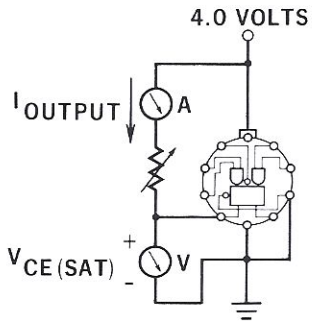
SCHEMATIC DIAGRAM OF 931 ELEMENT



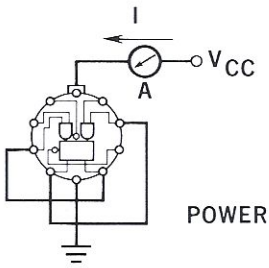
TEST CONDITIONS FOR FIGURES 1, 2, 3



TEST CONDITIONS FOR FIGURE 4

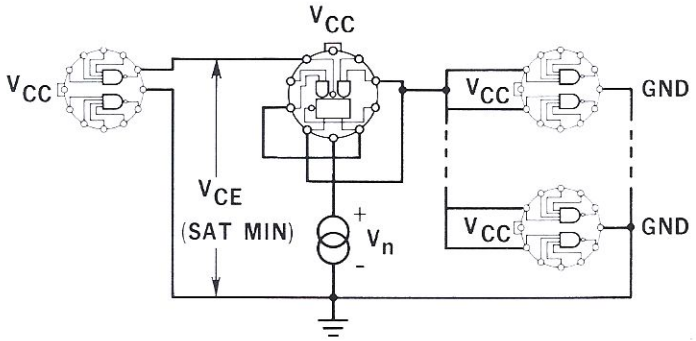


TEST CONDITIONS FOR FIGURE 5



POWER DRAIN = $I_A \times V_{CC}$

TEST CONDITIONS FOR FIGURES 6, 7, 8, 9



1. Refer to Fig. A. The "master" flip-flop stores the input information when the clock voltage becomes sufficiently positive to enable the input AND gate. The AND gate threshold voltage is given in Fig. 3 as a function of temperature. It is labeled $V_{AG\,th}$. Also given is the clock coupling transistor threshold voltage $V_{CP\,th}$. $V_{AG\,th}$ is an enabling voltage while $V_{CP\,th}$ is an inhibiting voltage. A rising clock voltage inhibits the clock coupling transistors at t_0 assuring that the "slave" flip-flop will not change. At t_1 the AND gates to the "master" flip-flop are enabled, storing the input information. A falling clock voltage disables the AND gates at t_2 preventing any further change in the "master" flip-flop. At t_3 the clock voltage falls below the inhibit level allowing the state of the "master" flip-flop to be transferred to the "slave" flip-flop.

2. Noise Immunity (Figs. 6-9)

There are two types of noise immunity which might be guaranteed: Signal noise or Ground noise

(A) Signal noise immunity

$$V_{NS} = \left| V_0(\max) - V_{0\,TH} \right|$$

or $$V_{NS} = \left| V_1(\min) - V_{1\,TH} \right|$$

where

$V_{OH} = V_1(\min)$	Minimum High Output Voltage
$V_{OL} = V_0(\max)$	Maximum Low Output Voltage
$V_{IH} = V_{1\,TH}$	Minimum High Input Voltage That Guarantees Proper Operation

$V_{IL} = V_{0\,TH}$ Maximum Low Input Voltage That Guarantees Proper Operation

(B) Ground noise immunity, V_{NG}. The worst case noise immunity for the 931 element is ground noise V_{NG}. The worst case positive ground noise immunity circuit condition will occur when the clock input is at the lowest V_{CE}(sat) voltage. For the noise immunity Graphs No. 6, 7, 8, and 9, the minimum saturation voltage was assumed to be +50 mV.

Note that the curves show two values of noise immunity at a given temperature. The low value of V_{CC} corresponds to a worst case beta limitation in the 931 element. The uppermost value corresponds to a V_{CE}(sat) limitation in the "slave" flip-flop. In Graph No. 8 for fan-out = 6 at -55°C, the worst case V_{NG} noise immunity is +300 mV at $V_{CC} \approx +4.20$ V. This corresponds to a worst case minimum signal noise immunity of >500 mV for the same fan-out, temperature, and power supply. Each of curves Fig. 6-9 shows V_n, the worst case of V_{NG} or V_{NS}.

Fig. 1
TYPICAL V_{OUT}-V_{CP} (CLOCK INPUT) TRANSFER CHARACTERISTIC

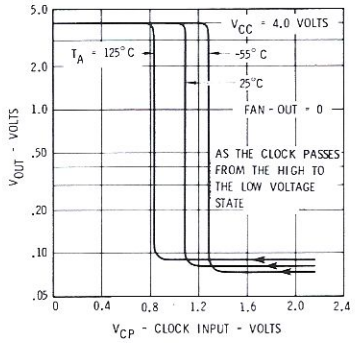

V_{CC} = 4.0 VOLTS
T_A = 125°C
-55°C
25°C
FAN-OUT = 0
AS THE CLOCK PASSES FROM THE HIGH TO THE LOW VOLTAGE STATE
V_{OUT} - VOLTS
V_{CP} - CLOCK INPUT - VOLTS

Fig. 2
TYPICAL V_{OUT}-V_{CP} (CLOCK INPUT) TRANSFER CHARACTERISTIC

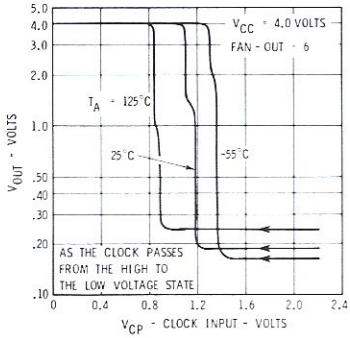

V_{CC} = 4.0 VOLTS
FAN-OUT = 6
T_A = 125°C
25°C
-55°C
AS THE CLOCK PASSES FROM THE HIGH TO THE LOW VOLTAGE STATE
V_{OUT} - VOLTS
V_{CP} - CLOCK INPUT - VOLTS

Fig. 3
TYPICAL THRESHOLD VOLTAGE VARIATION VERSUS TEMPERATURE FAN-OUT FROM n = 1 TO n = 9

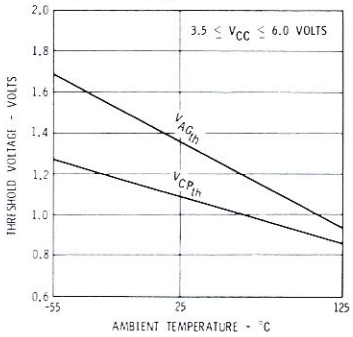


Fig. 4
OUTPUT SATURATION VOLTAGE VERSUS OUTPUT CURRENT TYPICAL

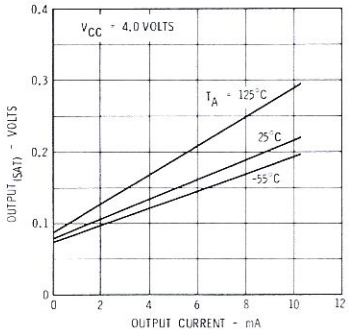


Fig. 5
POWER DISSIPATION VERSUS TEMPERATURE TYPICAL

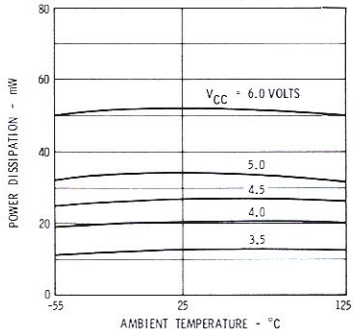


Fig. 6
SUPPLY VOLTAGE VERSUS TEMPERATURE FOR CONSTANT VALUES OF WORST CASE NOISE IMMUNITY

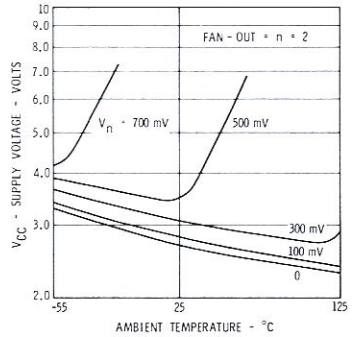


Fig. 7
SUPPLY VOLTAGE VERSUS TEMPERATURE FOR CONSTANT VALUES OF WORST CASE NOISE IMMUNITY

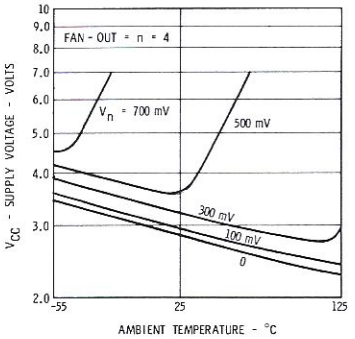


Fig. 8
SUPPLY VOLTAGE VERSUS TEMPERATURE FOR CONSTANT VALUES OF WORST CASE NOISE IMMUNITY

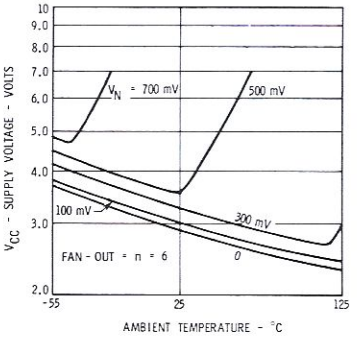
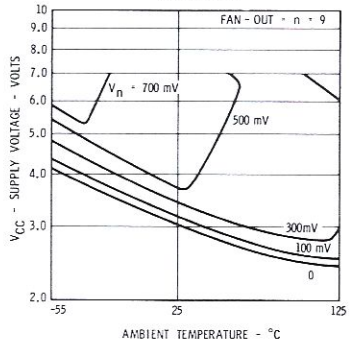
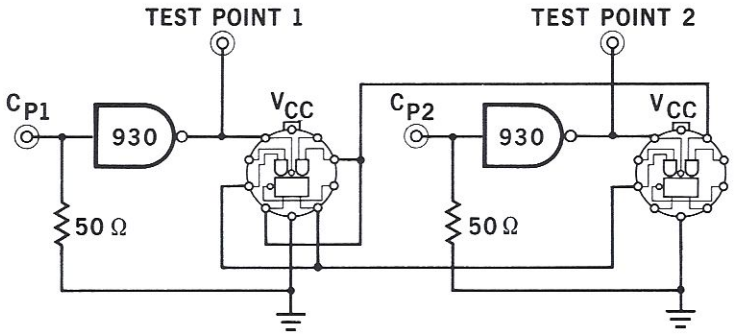
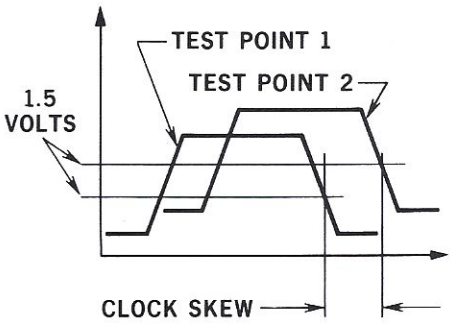


Fig. 9
SUPPLY VOLTAGE VERSUS TEMPERATURE FOR CONSTANT VALUES OF WORST CASE NOISE IMMUNITY



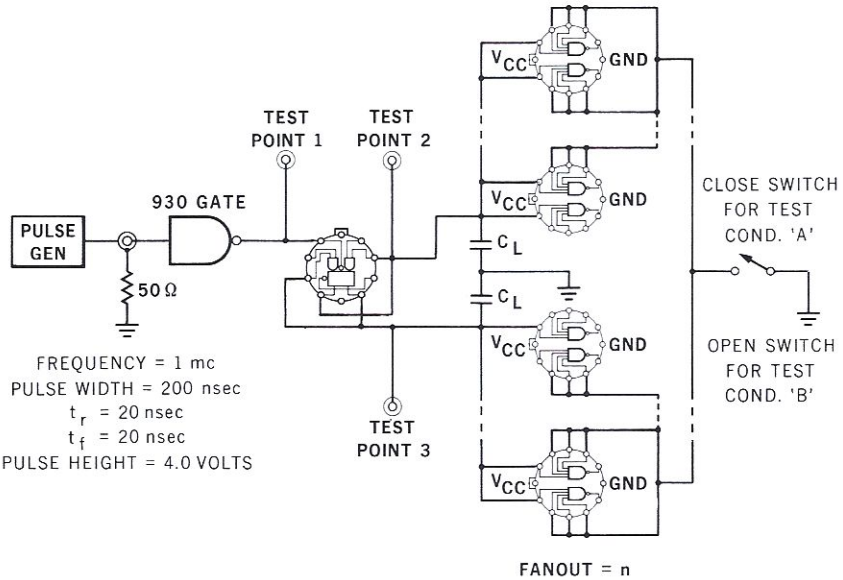
TEST CONDITIONS FOR FIGURE 10

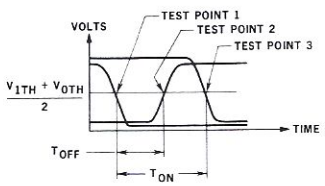




Clock skew is the maximum delay allowable between C_{P1} and C_{P2} which still results in reliably shifting information. Note that when C_{P2} occurs before C_{P1} there is no time delay restriction.

TEST CONDITIONS FOR FIGURES 11 THROUGH 27





NOTES:

1. In test condition 'A' fan-out = n, n-1 inputs are inactive and only one is active.
2. In test condition 'B', n inputs are active.
3. Both outputs are equally loaded. Only loading on output going positive has major effect except at low V_{CC} and low temperature. Refer to DTμL Composite Data Sheet, pages 4 and 5.

Fig. 10
TYPICAL ALLOWABLE CLOCK SKEW VERSUS TEMPERATURE

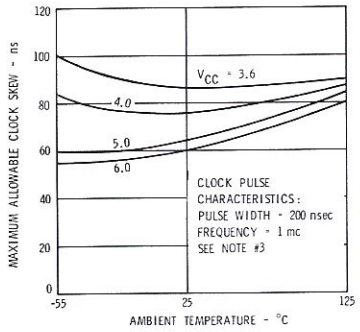


Fig. 11
MINIMUM CLOCK PULSE WIDTH REQUIRED TO SET AN 931 ELEMENT VERSUS TEMPERATURE — TYPICAL

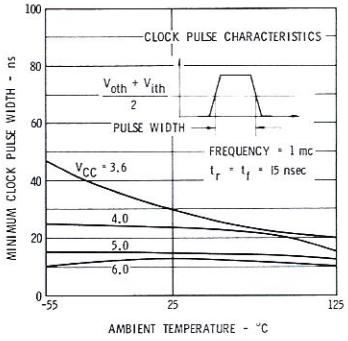


Fig. 12
T_{OFF} VERSUS TEMPERATURE FOR TEST CONDITION "A" 5 PF LOAD PER FAN-OUT ADDED

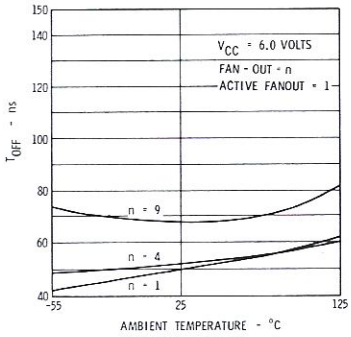


Fig. 13
T_{ON} VERSUS TEMPERATURE FOR TEST CONDITION "A" 5 PF LOAD PER FAN-OUT ADDED

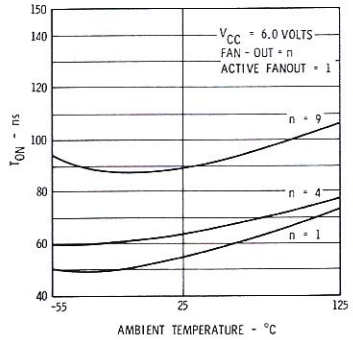


Fig. 14
T_{OFF} VERSUS TEMPERATURE FOR TEST CONDITION "A" 5 PF LOAD PER FAN-OUT ADDED

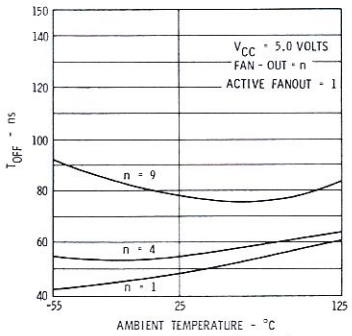


Fig. 15
T_{ON} VERSUS TEMPERATURE FOR TEST CONDITION "A" 5 PF LOAD PER FAN-OUT ADDED

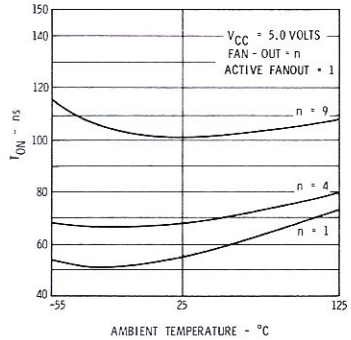


Fig. 16
T_{OFF} VERSUS TEMPERATURE FOR TEST CONDITION "A" 5 PF LOAD PER FAN-OUT ADDED

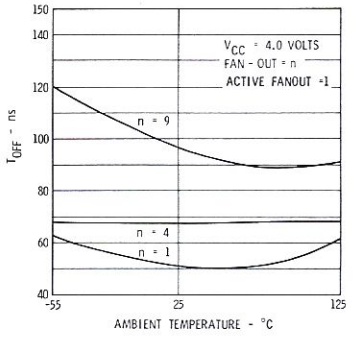


Fig. 17
T_{ON} VERSUS TEMPERATURE FOR TEST CONDITION "A" 5 PF LOAD PER FAN-OUT ADDED

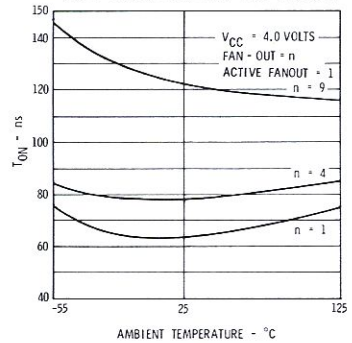


Fig. 18
T_{OFF} VERSUS TEMPERATURE FOR TEST CONDITION "A" 5 PF LOAD PER FAN-OUT ADDED

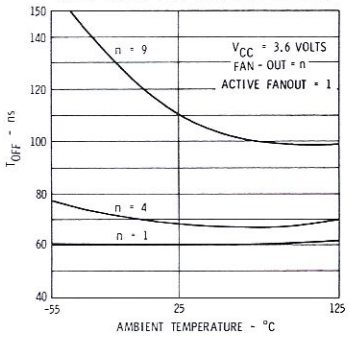


Fig. 19
T_{ON} VERSUS TEMPERATURE FOR TEST CONDITION "A" 5 PF LOAD PER FAN-OUT ADDED

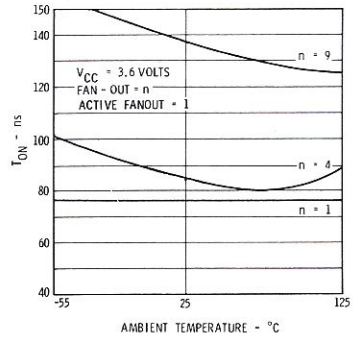


Fig. 20
T_{OFF} VERSUS TEMPERATURE FOR TEST CONDITION "B" 5 PF LOAD PER FAN-OUT ADDED

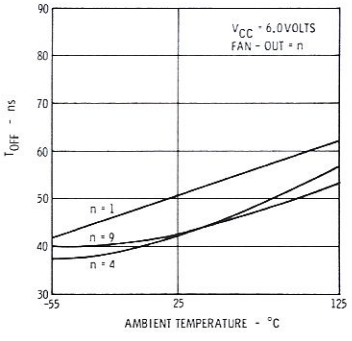


Fig. 21
T_{ON} VERSUS TEMPERATURE FOR TEST CONDITION "B" 5 PF LOAD PER FAN-OUT ADDED

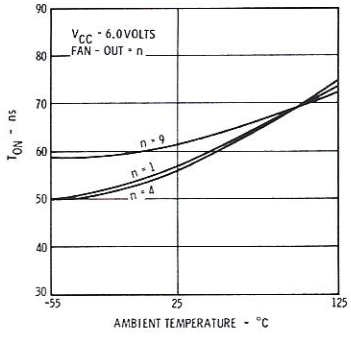


Fig. 22
T_{OFF} VERSUS TEMPERATURE FOR TEST CONDITION "B" 5 PF LOAD PER FAN-OUT ADDED

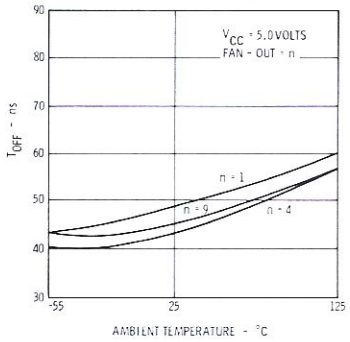


Fig. 23
T_{ON} VERSUS TEMPERATURE FOR TEST CONDITION "B" 5 PF LOAD PER FAN-OUT ADDED

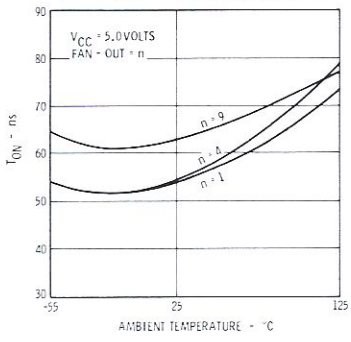


Fig. 24
T_{OFF} VERSUS TEMPERATURE FOR TEST CONDITION "B" 5 PF LOAD PER FAN-OUT ADDED

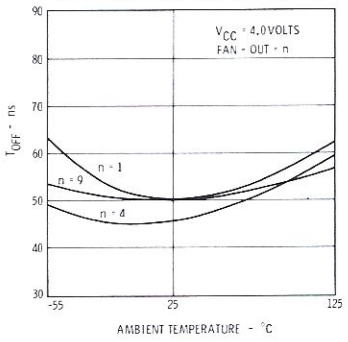


Fig. 25
T_{ON} VERSUS TEMPERATURE FOR TEST CONDITION "B" 5 PF LOAD PER FAN-OUT ADDED

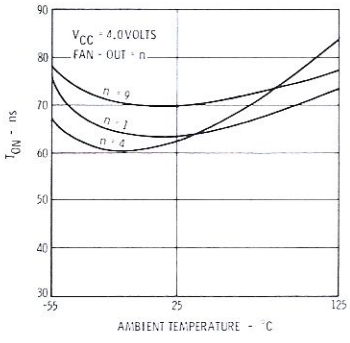


Fig. 26
T_{OFF} VERSUS TEMPERATURE FOR TEST CONDITION "B" 5 PF LOAD PER FAN-OUT ADDED

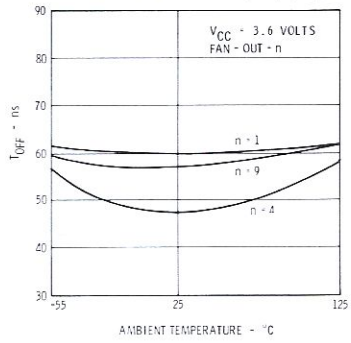
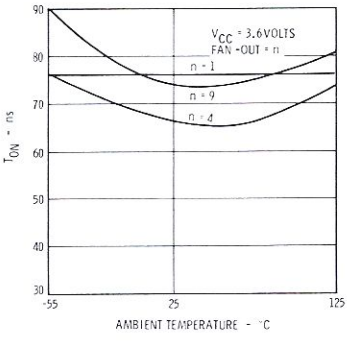
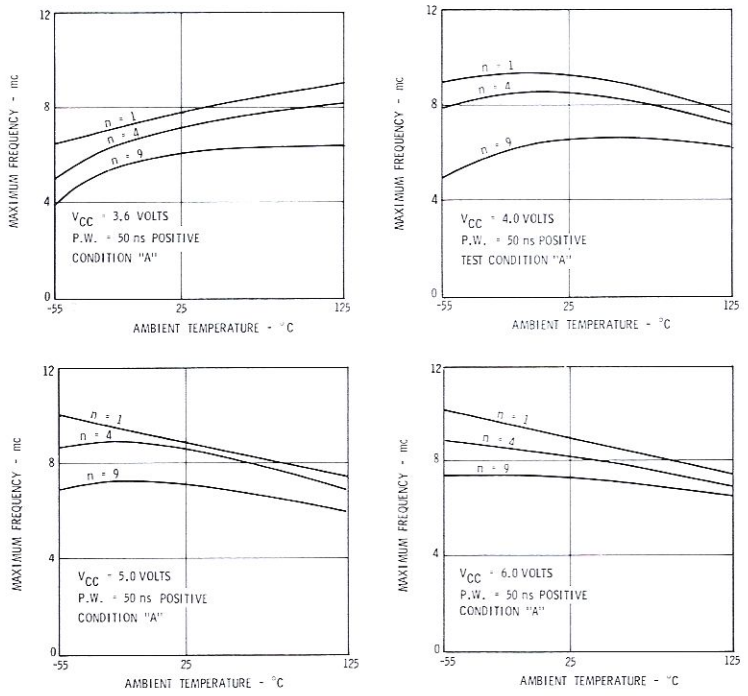


Fig. 27
T_{ON} VERSUS TEMPERATURE FOR TEST CONDITION "B" 5 PF LOAD PER FAN-OUT ADDED

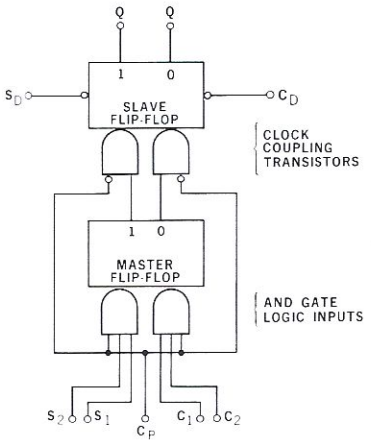


TYPICAL MAXIMUM FREQUENCY OF OPERATION VERSUS TEMPERATURE FOR A PULSE WIDTH OF 50nsec UNDER TEST CONDITION "A"
(5pf per fan-out)



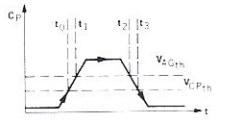
NOTE: Please refer to DTμL Composite Data Sheet, pages 4 and 5, for Capacitive loading effects and improvements with resistor shunting to V_{CC}.

FIG. A. EXPLANATION OF FIG. 3 $V_{AG_{th}}$ and $V_{CP_{th}}$.
(See note 1 for operation and terminology.)



CLOCK TIMING SEQUENCE

- t_0 - Turn off clock coupling transistors.
- t_1 - Enter logic into master FLIP-FLOP
- t_2 - Inhibit AND GATE input to master
- t_3 - Transfer information from master into slave.



APPLICATION DATA

The DTμL-931 Clocked Flip-Flop is a complete, self-sufficient, clocked storage element. It is directly coupled throughout and hence, does not depend on capacitors, propagation delays, or charge storage effects to achieve reliable time separation and retention of input logic values. As a direct consequence, its inputs are not sensitive to rise or fall times of logic signals, nor to pulse widths. It responds exclusively to input voltage levels with definite, separated thresholds for both the low and high input voltage levels.

Two types of data entry are possible: Synchronous, requiring the concurrence of an active voltage level at the trigger input as well as the associated synchronous input, and asynchronous, requiring nothing more than the active signal level at the appropriate asynchronous inputs.

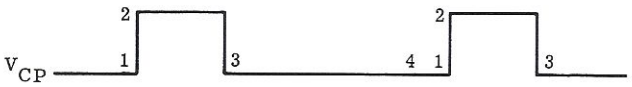
Synchronous Entry

The entry of information at the synchronous inputs, set (S) and clear (C), is under direct control of the trigger (T) input. Input signals formed at the input AND gates are entered into the first of two simple latch circuits, hereafter referred to as "master" and "slave," when the trigger input is high, and thereafter transferred to the "slave" when the trigger input becomes low. The "slave" outputs are the outputs for the aggregate unit. The synchronous inputs are inhibited during the time interval when the outputs of Clocked Flip-Flops are changing, thus preventing more than one change in output for each cycle of the trigger input from low to high and back.

The state of the "master" just prior to the negative excursion of the trigger signal represents the condition which the "slave" outputs will assume. The constraints placed upon the synchronous inputs while the trigger level is high are: The inputs must be settled and stable for a sufficient time to permit the "master" to assume a definite condition, and the inputs must not be simultaneously active (high). To permit unrestricted use of the input AND gates, a necessary and sufficient condition for trouble-free operation is that synchronous logic inputs may change only while the trigger input signal is low.

Waveform Below

1. Synchronous logic inputs stable
2. Enter "master"
3. Transfer "master" to "slave"
4. Propagate through logic gates



Asynchronous Entry

Asynchronous Entry is made at the "slave." Therefore, it is clear that one cannot use the asynchronous inputs without regard for the synchronous inputs if well-defined operation is to result. The trigger input must be high during asynchronous entry so that the "master" outputs will not conflict with the asynchronous inputs.

The necessity for a high trigger input during asynchronous entry precludes use of the asynchronous inputs when the trigger signal for each stage is not under complete control except for certain specific conditions. For example, a ripple-carry counter, where the trigger input of each stage is connected to an output of the previous stage. Here, because, of the signal polarities involved, it is only possible to clear all "slaves" if the counter is a reverse counter or set all "slaves" if it is a forward counter. In neither case is it possible to set an arbitrary pattern reliably.

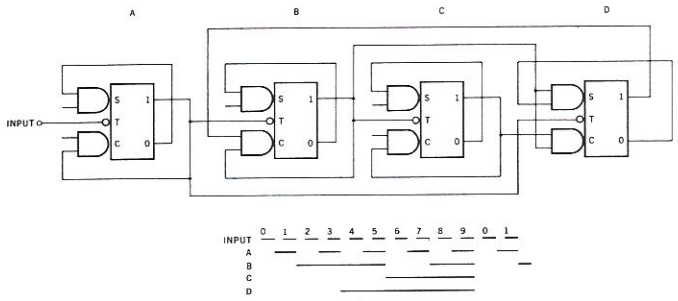
Arbitrary asynchronous entry to shift registers is straightforward because the shift signal (trigger input) may be held high at will. Due to the direct connection between the "slave" of one stage and the "master" of its successor, the information entered into the "slave" of one stage will automatically be transferred to the "master" of the next. Therefore, the next negative excursion of the shift pulse will result in shifting information one stage - the desired response. At the input stage to the shift register, where serial information originates, care must be exercised to insure that the initial "master" flip-flop is set to the proper condition, corresponding to the next bit of information that is to appear in this stage.

A general consideration in asynchronous entry is propagation time. After modifying the state of "slaves" asynchronously, adequate time must be allotted for signal propagation through all intervening logic networks before resuming synchronous operation. Furthermore, signal races due to different signal path lengths become a possibility.

Since asynchronous entry condones changing logic inputs during the time that trigger input signals are high - an otherwise forbidden situation in a synchronous system - particular care is required when both of the Clocked Flip-Flop AND gate inputs are used. A common case is J-K mode operation (stage outputs cross-connected to their own inputs). Here, one input AND gate is always inhibited; and, while the other input can cause the "master" flip-flop to change, the inhibited input cannot return the "master" to its initial state if the final input value does not indicate that a change of the overall state is required. Thus, when the clock input next goes low, transferring "master" to "slave," an erroneous output can ensue.

Similar remarks apply to more complex interconnections, and the designer should always assure himself that asynchronous entry does not create a conflict in some unsuspected way.

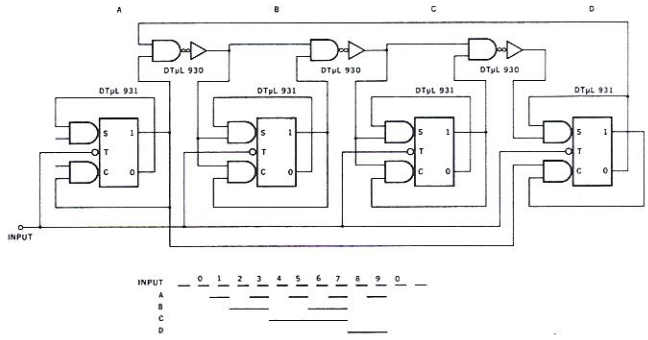
1-2-4-2 DECADE USING DTμL 931 CLOCKED FLIP-FLOPS



COUNT SEQUENCE			
A	B	C	D
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	0
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	1
1	1	1	1
0	0	0	0

etc.

SYNCHRONOUS SERIAL CARRY 1-2-4-8 DECADE



COUNT SEQUENCE			
A	B	C	D
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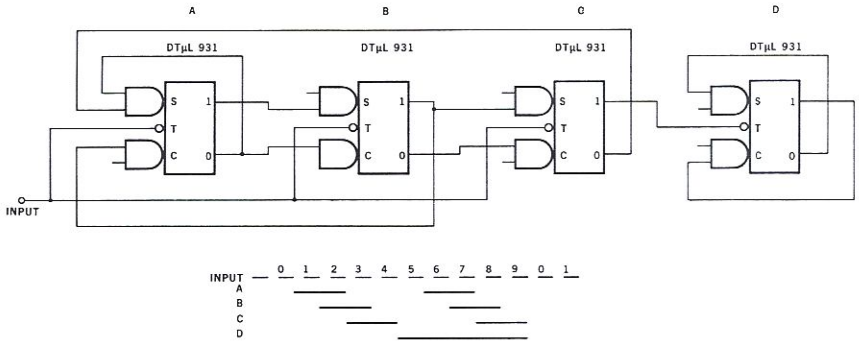
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	0
0	0	0	1
1	0	0	1
0	0	0	0

etc.

CODED BIQUINARY DECADE COUNTER



COUNT SEQUENCE			
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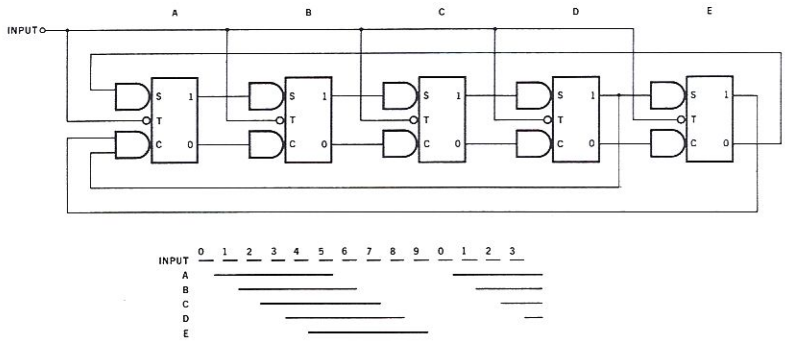
0	1	1	0
0	0	1	0
0	0	0	1
1	0	0	1
1	1	0	1
0	1	1	1
0	0	1	1
0	0	0	0

etc.

MODULO-10 SHIFT COUNTER USING DTμL931'S



COUNT SEQUENCE				
A	B	C	D	E
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1	0	0	0	0
1	1	0	0	0
1	1	1	0	0
1	1	1	1	0
1	1	1	1	1
0	1	1	1	1
0	0	1	1	1
0	0	0	1	1
0	0	0	0	1
0	0	0	0	0

etc.

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